WHAT IS CLAIMED IS:

1. A multiprocessor system comprising:

a master processor that issues commands;

a plurality of processor-elements, each of which has a local memory and a first command pooling buffer, the first command pooling buffer pooling the commands issued from the master processor, wherein the processor-elements are controlled by the commands in the buffer;

a global memory which is common to the master processor and the processor-elements;

a transfer device having a second command pooling buffer, the transfer device being controlled by some of the commands issued from the master processor, to transfer a program/data between the local memory of the processor-elements and the global memory, wherein the commands are pooled in the second command pooling buffer; and

a counter device to notify the master processor that the number of responses to the commands issued from the master processor, returned from the processor-elements and transfer device, has reached a predetermined number of responses, the predetermined number being pre-stored in the counter device.

2. The system according to claim 1, wherein the transfer device includes a direct memory access (DMA) controller.

3. The system according to claim 1, wherein the master processor issues the commands for controlling both transfer device and processor-elements by a multithreaded program.

4. The system according to claim 3, wherein the commands include a first command together with a first thread identifier and a second command together with a second thread identifier, the first and second thread identifiers being generated according to the multithreaded program.

5. The system according to claim 1, wherein the second command pooling buffer of the transfer device includes:

a program local storage (PLS) command table; and

a data local storage (DLS) command table.

6. The system according to claim 5, wherein the transfer device includes:

a statemachine configured to manage an execution of a program local storage command, wherein the command specifies a transfer of a program from the master processor to one of the processor-elements and the command is acquired from the program local storage command table, and configured to manage an execution of a data local storage command, wherein the command specifies a transfer of data from the master processor to one of the processor-elements and the data is acquired from the data local storage

command table.

7. The system according to claim 6, further comprising:

a program local storage managing table, to be referred by the statemachine, for managing the local memory of the corresponding one of the processor-elements; and

a data local storage managing table, to be referred by the statemachine, for managing the local memory of the corresponding one of the processor-elements.

8. The system according to claim 7, wherein each of the processor-elements executes the program transferred to the local memory after confirming that the data to be used by the program is prepared in the local memory by referring to the data local storage managing table.

9. The system according to claim 1, wherein the master processor issues the commands continuously.

10. The system according to claim 1, wherein the counter device counts the responses from the processor-elements and transfer device.

11. The system according to claim 1, wherein the predetermined number is at least more than 2.

12. A control method for controlling the operation of a multiprocessor system including: a master processor; at least one processor-element having a

program local memory and a data local memory; a global memory which is common to the master processor and processor-element; and a transfer device, the method comprising:

continuously issuing a plurality of commands by the master processor;

transferring a program from the global memory to the program local memory by the transfer device in accordance with one of the commands;

transferring a data from the global memory to the data local memory by the transfer device in accordance with another one of the commands;

executing the program by the processor-element, the processor-element referring to the program local memory and data local memory in accordance with still another one of the commands;

transferring the execution result of the program from the data local memory to the global memory by the transfer device in accordance with still another one of the commands; and

notifying the master processor that the number of responses to the commands issued from the master processor, returned from the processor-element and transfer device, has reached a predetermined number of responses, the predetermined number being pre-stored.

13. The method according to claim 12, wherein the transfer device includes a direct memory access (DMA)

controller.

14. The method according to claim 12, wherein the master processor issues the commands for controlling the transfer device and processor-element by a multithreaded program.

15. The method according to claim 14, wherein the commands include a first command together with a first thread identifier and a second command together with a second thread identifier, the first and second thread identifiers being generated according to the multithreaded program.

16. The method according to claim 12, wherein the processor-element executes the program transferred to the program local memory after confirming that the data to be used by the program is prepared in the data local memory by referring to a data local storage managing table.

17. The method according to claim 12, wherein the master processor issues the commands continuously.

18. The method according to claim 12, wherein the predetermined number is at least more than 2.